CLAIMS

What is claimed is:

1. A method comprising:

generating a write strobe signal to latch output data into a memory unit comprising one or more dual data rate synchronous dynamic random access memory (DDR-SDRAM) devices, the write strobe signal having an edge transition at approximately the center of a data window corresponding to the output data; and

delaying a first receive clock signal by a first delay period using a delay locked loop (DLL) circuit to generate a first delayed receive clock signal, the first delayed receive clock signal being used to latch incoming data from the memory unit.

2. The method of claim 1 further comprising:

aligning the edge transition of the write strobe signal and the data window corresponding to the output data such that the edge transition of the write strobe signal approximately corresponds to the center of the data window.

3. The method of claim 2 wherein aligning comprises:

driving the output data in response to the rising edge transitions of first and second clock signals, respectively, the first and second clock signals being phase shifted by one half of a clock period corresponding to the frequency of the first and second clock signals; and

driving the write strobe signal in response to the rising edge transitions of third and fourth clock signals, respectively, the third and fourth clock signals being phase

shifted by one half of the clock period, the third clock signal being phase shifted by approximately one quarter of the clock period with respect to the first clock signal, the output data and the write strobe signal having approximately the same clock to output time.

4. The method of claim 3 wherein the first, second, third, and fourth clock signals are derived from a system clock signal using a phase locked loop (PLL) circuit.

5. The method of claim 3 wherein the first receive clock signal is derived from the first clock signal, the first receive clock signal being delayed relative to the first clock signal to approximately match the flight time of the incoming data.

6. The method of claim 1 wherein the first delay period is used to provide sufficient setup time and hold time for latching the incoming data in response to the transition of the first delayed receive clock signal.

7. The method of claim 1 wherein the DLL circuit is programmable via a register.

8. The method of claim 7 wherein the first delay period corresponds to a value stored in the register.

9. The method of claim 1 further comprising:

delaying a second receive clock signal by the first delay period using the delay locked loop (DLL) circuit to generate a second delayed receive clock signal, the second

delayed receive clock signal being used to latch incoming data from the memory unit, the second receive clock signal being phase shifted by one half of a clock period with respect to the first receive clock signal.

10. An apparatus comprising:

logic to generate a write strobe signal that is used to latch outgoing data into a memory unit comprising one or more DDR-SDRAM devices, the write strobe signal having an edge transition at approximately the center of a data window corresponding to the outgoing data; and

logic to delay a first receive clock signal by a first delay period using a delay locked loop (DLL) circuit to generate a first delayed receive clock signal, the first delayed receive clock signal being used to latch incoming data from the memory unit.

11. The apparatus of claim 10 further comprising:

logic to align the edge transition of the write strobe signal and the data window corresponding to the outgoing data such that the edge transition of the write strobe signal approximately corresponds to the center of the data window.

12. The apparatus of claim 11 wherein the logic to align comprises:

first and second latching devices to latch the outgoing data in response to transitions of first and second clock signals, respectively, the first and second clock signals being phase shifted by one half of a clock period corresponding to the frequency of the first and second clock signals; and

third and fourth latching devices to latch the write strobe signal in response to transitions of third and fourth clock signals, respectively, the third and fourth clock signals being phase shifted by one half of the clock period, the third clock signal being phase shifted by one quarter of the clock period with respect to the first clock signal.

13. The apparatus of claim 12 wherein the first, second, third, and fourth clock signals are derived from a system clock signal using a phase locked loop (PLL) circuit.

14. The apparatus of claim 12 wherein the first receive clock signal is derived from the first clock signal, the first receive clock signal being delayed relative to the first clock signalto approximately match the flight time of the incoming data.

15. The apparatus of claim 10 wherein the first delay period is used to provide sufficient setup time and hold time for latching the incoming data in response to the transition of the first delayed receive clock signal.

16. The apparatus of claim 10 wherein the DLL circuit is programmable via a register.

17. The apparatus of claim 16 wherein the first delay period corresponds to a value stored in the register.

18. The apparatus of claim 10 further comprising:

logic to delay a second receive clock signal by the first delay period using the DLL circuit to generate a second delayed receive clock signal, the second delayed receive

clock signal being used to latch incoming data from the memory unit, the second receive clock signal being phase shifted by approximately one half of a clock period with respect to the first receive clock signal.

19. A system comprising:

a memory unit comprising one or more DDR-SDRAM devices; and

a graphics accelerator coupled to the memory unit, comprising:

a memory interface to control data transfer between the graphics accelerator and the memory unit, comprising:

logic to generate a write strobe signal that is used to latch outgoing data into the memory unit comprising one or more DDR-SDRAM devices, the write strobe signal having an edge transition at approximately the center of a data window corresponding to the outgoing data; and

logic to delay a first receive clock signal by a first delay period using a delay locked loop (DLL) circuit to generate a first delayed receive clock signal, the first delayed receive clock signal being used to latch incoming data from the memory unit.

20. The system of claim 19 wherein the memory interface comprises:

logic to align the edge transition of the write strobe signal and the data window corresponding to the outgoing data such that the edge transition of the write strobe signal approximately corresponds to the center of the data window.

21. The system of claim 20 wherein the logic to align comprises:

first and second latching devices to latch the outgoing data in response to transitions of first and second clock signals, respectively, the first and second clock signals being phase shifted by one half of a clock period corresponding to the frequency of the first and second clock signals; and

third and fourth latching devices to latch the write strobe signal in response to transitions of third and fourth clock signals, respectively, the third and fourth clock signals being phase shifted by one half of the clock period, the third clock signal being phase shifted by one quarter of the clock period with respect to the first clock signal.

22. The system of claim 19 wherein the first delay period is used to provide sufficient setup time and hold time for latching the incoming data in response to the transition of the first delayed receive clock signal.

23. The system of claim 19 wherein the DLL circuit is programmable via a register.

24. The system of claim 23 wherein the first delay period corresponds to a value stored in the register.

25. The system of claim 19 wherein the memory interface further comprises:

logic to delay a second receive clock signal by the first delay period using the DLL circuit to generate a second delayed receive clock signal, the second delayed receive clock signal being used to latch incoming data from the memory unit, the second receive

clock signal being phase shifted by approximately one half of a clock period with respect to the first receive clock signal.